Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the present application:

Listing of Claims:

Claim 1 (currently amended): An imager cell including a substrate connected to a voltage, the imager cell comprising:

a photoreceptor;

a sense node; and

a pinned transfer gate disposed between the photoreceptor and the sense node, the pinned transfer gate being connected to the voltage and further being configured to transfer charge between the photoreceptor and the sense node.

Claim 2 (original): An imager cell as defined in claim 1, wherein the pinned transfer gate comprises a p-doped pinned region in an n-doped transfer region.

Claim 3 (original): An imager cell as defined in claim 1, further comprising a photoreceptor readout gate disposed above the photoreceptor.

Claim 4 (original): An imager cell as defined in claim 1, wherein the photoreceptor comprises a photogate.

Claim 5 (original): An imager cell as defined in claim 1, wherein the photoreceptor comprises a photodiode.

Claim 6 (original): An imager cell as defined in claim 1, further comprising a reset transistor disposed to reset the sense node.

Claim 7 (original): An imager cell as defined in claim 1, further comprising an output amplifier coupled to the sense node.

Claim 8 (original): An imager cell as defined in claim 7, wherein the output amplifier is a source follower amplifier.

Claim 9 (original): An imager cell as defined in claim 3, further comprising a readout clock connection coupled to the photoreceptor readout gate.

Claim 10 (original): An imager cell as defined in claim 9, further comprising control circuitry coupled to the readout clock connection, the control circuitry supplying a photoreceptor readout clock.

Claim 11 (original): An imager cell as defined in claim 10, wherein the photoreceptor readout clock is characterized by a V+ level applied during an integration period, and a V- level applied during a transfer period.

Claim 12 (currently amended): An imager cell including a substrate connected to a voltage, the imager cell comprising:

a photoreceptor;

a sense node;

a pinned transfer gate disposed between the photoreceptor and the sense node, the pinned transfer gate being connected to the voltage and further being configured to transfer charge between the photoreceptor and the sense node; and

a photoreceptor readout gate disposed above the photoreceptor, the photoreceptor readout gate having material removed to form a photoreceptor readout gate light aperture above the photoreceptor, whereby the photoreceptor provides enhanced response to blue light.

Claim 13 (original): An imager cell as defined in claim 12, further comprising a pinned aperture region under the photoreceptor readout gate light aperture.

Claim 14 (original): An imager cell as defined in claim 12, wherein the pinned transfer gate comprises a p-doped pinned region in an n-doped transfer region.

Claim 15 (original): An imager cell as defined in claim 12, wherein the photoreceptor comprises a photo gate.

Claim 16 (original): An imager cell as defined in claim 12, wherein the photoreceptor comprises a photodiode.

Claim 17 (original): An imager cell as defined in claim 12, further comprising a reset transistor disposed to reset the sense node.

Claim 18 (original): An imager cell as defined in claim 12, further comprising an output amplifier coupled to the sense node.

Claim 19 (original): An imager cell as defined in claim 18, further comprising an anti-reflective coating disposed above the photoreceptor.

Claim 20 (original): An imager cell as defined in claim 12, further comprising a readout clock connection coupled to the photoreceptor readout gate.

Claim 21 (original): An imager cell as defined in claim 20, further comprising control circuitry coupled to the readout clock connection, the control circuitry supplying a photoreceptor readout clock.

Claim 22 (original): An imager cell as defined in claim 21, wherein the photoreceptor readout clock is characterized by a V+ level applied during an integration period, and a V- level applied during a transfer period.

Claim 23 (currently amended): An imager cell including a substrate connected to a voltage, the imager cell comprising:

a photoreceptor;

a sense node;

a pinned transfer gate disposed between the photoreceptor and the sense node, the pinned transfer gate being connected to the voltage and further being configured to transfer charge between the photoreceptor and the sense node; and

a photoreceptor readout gate disposed above the photoreceptor, the photoreceptor readout gate characterized by a photoreceptor readout gate thickness of less than 2000 Angstroms, whereby the photoreceptor provides enhanced response to blue light.

Claim 24 (original): An imager cell as defined in claim 23, wherein the photoreceptor readout gate thickness is less than 1000 Angstroms.

Claim 25 (original): An imager cell as defined in claim 23, wherein the photoreceptor readout gate thickness is less than 500 Angstroms.

Claim 26 (original): An imager cell as defined in claim 23, wherein the pinned transfer gate comprises a p-doped pinned region in an n-doped transfer region.

Claim 27 (original): An imager cell as defined in claim 23, wherein the photoreceptor comprises a photogate.

Claim 28 (original): An imager cell as defined in claim 23, wherein the photoreceptor comprises a photodiode.

Claim 29 (original): An imager cell as defined in claim 23, further comprising a reset transistor disposed to reset the sense node.

Claim 30 (original): An imager cell as defined in claim 23, further comprising an output amplifier coupled to the sense node.

Claim 31 (original): An imager cell as defined in claim 28, wherein the output amplifier is a source follower amplifier.

Claim 32 (original): An imager cell as defined in claim 23, further comprising a readout clock connection coupled to the photoreceptor readout gate.

Claim 33 (original): An imager cell as defined in claim 32, further comprising control circuitry coupled to the readout clock connection, the control circuitry supplying a photoreceptor readout clock.

Claim 34 (original): An imager cell as defined in claim 33, wherein the photoreceptor readout clock is characterized by a V+ level applied during an integration period, and a V- level applied during a transfer period.

Claim 35-57 (cancelled).

Claim 58 (currently amended): An imager cell including a substrate connected to a voltage, the imager cell comprising:

means for detecting incident photons;

means for storing transferred charge for readout; and

a pinned transfer gate disposed between the means for detecting and the means for storing, the pinned transfer gate being connected to the voltage and further being configured to transfer charge between the means for detecting and the means for storing.

Claim 59 (original): An imager cell as defined in claim 58, wherein the pinned transfer gate comprises a p-doped pinned region in an n-doped transfer region.

Claim 60 (original): An imager cell as defined in claim 58, further comprising means for transferring charge from the means for detecting incident photons to the pinned transfer gate.

Claim 61 (original): An imager cell as defined in claim 58, further comprising means for resetting the means for storing transferred charge.

Claim 62 (original): An imager cell as defined in claim 58, further comprising means for amplifying the transferred charge.

Claim 63 (original): An imager cell as defined in claim 60, further comprising means for clocking the means for transferring charge.

Claim 64 (original): An imager cell as defined in claim 63, wherein the means for clocking is characterized by a V+ level applied during an integration period, and a V- level applied during a readout transfer period.

Claim 65 (original): An imager cell as defined in claim 60, wherein the means for transferring charge comprises a photoreceptor readout gate characterized by a thickness of less than 2000 Angstroms.

Claim 66 (original): An imager cell as defined in claim 61, wherein the means for transferring charge comprises a photoreceptor readout gate characterized by a thickness of less than 1000 Angstroms.

Claim 67 (original): An imager cell as defined in claim 61, wherein the means for transferring charge comprises a photoreceptor readout gate characterized by a thickness of less than 500 Angstroms.

Claim 68 (original): An imager cell as defined in claim 60, wherein the means for transferring charge comprises a photoreceptor readout gate having material removed to form a photoreceptor readout gate light aperture above the means for detecting incident photons.

Claim 69 (original): An imager cell as defined in claim 68, further comprising a pinned aperture region under the photoreceptor readout gate light aperture.

Claim 70 (currently amended): An imaging array including a substrate connected to a voltage, the imaging array comprising:

an array of imager cells, each imager cell comprising a photoreceptor, a sense node, and a photoreceptor readout gate; and wherein at least one of the imager cells further comprises a pinned transfer gate disposed between the photoreceptor and the sense node, the pinned transfer gate being connected to the voltage and further being configured to transfer charge between the photoreceptor and the sense node; and

control circuitry coupled to each photoreceptor readout gate for supplying a photoreceptor readout clock simultaneously to a set of photoreceptors in the array,

whereby accumulated charge in each photoreceptor is transferred to its sense node to provide a snapshot of an image acquired by the imaging array.

Claim 71 (currently amended): An imager cell including a substrate connected to a voltage, the imager cell comprising:

a photoreceptor including a photoreceptor readout gate;

a sense node;

a pinned transfer gate disposed between the photoreceptor and the sense node, the pinned transfer gate being connected to the voltage and further being configured to transfer charge between the photoreceptor and the sense node; and

control circuitry coupled to the photoreceptor readout gate for applying a photoreceptor readout clock to the photoreceptor readout gate, the photoreceptor readout

clock comprising an integration period characterized by an integration voltage selected from a plurality of predetermined integration voltages to setup a preselected charge capacity level in the photoreceptor.